

SIHAO LIU

Research Scientist, Architecture Research Group, NVIDIA Research

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RESEARCH INTERESTS

- Programmable spatial accelerators, hardware/software co-design, compilers, and on-chip interconnects.
- Agentic chip architecture and electronic design automation; independently reviewed and executable engineering workflows.

EDUCATION

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|------|---|---------------------------------------|
| 2026 | <ul style="list-style-type: none">• Ph.D. in Computer Science <p><i>Degree awarded September 2026. Advisor: Tony Nowatzki.</i>
Dissertation: Loom: Full-Stack Compilation and Automated Exploration of Heterogeneous Multi-Core Spatial Accelerator Systems.</p> | University of California, Los Angeles |
| 2021 | <ul style="list-style-type: none">• M.S. in Computer Science | University of California, Los Angeles |
| 2019 | <ul style="list-style-type: none">• B.Eng. in Electrical Engineering | Xi'an Jiaotong University |

PROFESSIONAL EXPERIENCE

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| 09/2026–
present | <ul style="list-style-type: none">• Research Scientist — NVIDIA Research
Architecture Research Group. Research on next-generation chip architectures and agentic systems for hardware design. |
| 06/2022–
10/2023 | <ul style="list-style-type: none">• Hardware Engineering Intern — SiFive
Memory management unit ownership; load/store and cache subsystem design and verification. Full-time summer and part-time academic-year appointments. |

ACADEMIC EXPERIENCE

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| 2019–2026 | <ul style="list-style-type: none">• Doctoral Researcher — UCLA PolyArch Research Group |
| 2018 | <ul style="list-style-type: none">• Undergraduate Researcher (summer) — UCLA PolyArch Research Group |
| 2017 | <ul style="list-style-type: none">• Visiting Scholar (summer) — University of Lausanne
Neuroheuristic Research Group. Supervisor: Alessandro E. P. Villa. |

RESEARCH PROJECTS AND OPEN SOURCE

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| 2026 | <ul style="list-style-type: none">• Loom. A compiler and exploration framework for heterogeneous multi-core spatial accelerators, connecting a shared hardware model, compilation, simulation, and reproducible evaluation. |
| Open
source | <ul style="list-style-type: none">• Humanize / Humanfia. I created Humanize 1 at UCLA: an implementation and independent-review loop for coding agents. I am a founding member of Humanfia, where we extend this approach to longer engineering tasks. |
| 2026 | <ul style="list-style-type: none">• gem5 build-system migration. Migration of gem5's SCons build to CMake and Ninja with a Bazel overlay (567 files, 133 commits), produced by a Humanize builder-reviewer loop and validated by full builds, unit tests, and matching simulation objects; awaiting upstream review. |
| 2025–2026 | <ul style="list-style-type: none">• OverNoC / BenchNoC. Characterization of hardened FPGA networks-on-chip and hierarchical network overlays for multi-chiplet reconfigurable systems. |
| 2020–2022 | <ul style="list-style-type: none">• DSAGEN / OverGen. Automated generation of programmable spatial architectures and FPGA overlays, bringing compilation, hardware implementation, and design-space exploration into one flow. |

RESEARCH IMPACT

913 citations; h-index 11; i10-index 11. Google Scholar snapshot, September 29, 2026.

CONFERENCE PUBLICATIONS

* Equal contribution. Preprints and the dissertation are listed separately.

- FCCM 2025 • H. Ke, **S. Liu**, L. Guo, Z. He, L. Song, S. Basalama, Y. Chi, T. Nowatzki, J. Cong. NoH: NoC Compilation in High-Level Synthesis.
- MICRO 2022 • **S. Liu**^{*}, J. Weng^{*}, D. Kupsh, A. Sohrabizadeh, Z. Wang, L. Guo, J. Liu, M. Zhulin, R. Mani, L. Zhang, J. Cong, T. Nowatzki. OverGen: Improving FPGA Usability through Domain-Specific Overlay Generation. **Best Paper Runner-up**.
- HPCA 2022 • Z. Wang, J. Weng, **S. Liu**, T. Nowatzki. Near-Stream Computing: General and Transparent Near-Cache Acceleration.
- ISCA 2021 • V. Dadu, **S. Liu**, T. Nowatzki. PolyGraph: Exposing the Value of Flexibility for Graph Processing Accelerators. **IEEE Micro Top Picks 2022**.
- ISCA 2020 • J. Weng^{*}, **S. Liu**^{*}, V. Dadu, Z. Wang, P. Shah, T. Nowatzki. DSAGEN: Synthesizing Programmable Spatial Accelerators. **IEEE Micro Top Picks 2021, Honorable Mention**.
- HPCA 2020 • J. Weng, **S. Liu**, Z. Wang, V. Dadu, T. Nowatzki. A Hybrid Systolic-Dataflow Architecture for Inductive Matrix Algorithms.
- MICRO 2019 • V. Dadu, J. Weng, **S. Liu**, T. Nowatzki. Towards General Purpose Acceleration by Exploiting Common Data-Dependence Forms. **IEEE Micro Top Picks 2020**.
- MICRO 2019 • A. Sharifian, R. Hojabr, N. Rahimi, **S. Liu**, A. Guha, T. Nowatzki, A. Shriraman. μ IR: An Intermediate Representation for Transforming and Optimizing the Microarchitecture of Application Accelerators.
- IUS 2017 • S. Zhang, S. Shang, Y. Han, R. Xu, **S. Liu**, L. Zhang, S. Wu, G. Niu, S. Wang, M. Wan. Monitoring of Microwave Ablation in Porcine Liver Using Ultrasonic Nakagami Imaging.

JOURNAL PUBLICATIONS

- Micro 2022 • J. Weng, **S. Liu**, D. Kupsh, T. Nowatzki. Unifying Spatial Accelerator Compilation With Idiomatic and Modular Transformations.
IEEE Micro, 42(5), 59-69.
- Micro 2022 • V. Dadu, **S. Liu**, T. Nowatzki. Systematically Understanding Graph Accelerator Dimensions and the Value of Hardware Flexibility.
IEEE Micro, 42(4), 87-96.
- Micro 2020 • V. Dadu, J. Weng, **S. Liu**, T. Nowatzki. Towards General-Purpose Acceleration: Finding Structure in Irregularity.
IEEE Micro, 40(3), 37-46.
- CAL 2019 • J. Weng, **S. Liu**, V. Dadu, T. Nowatzki. DAEGEN: A Modular Compiler for Exploring Decoupled Spatial Accelerators.
IEEE Computer Architecture Letters, 18(2), 161-165.
- TMI 2018 • S. Zhang, S. Shang, Y. Han, C. Gu, S. Wu, **S. Liu**, G. Niu, A. Bouakaz, M. Wan. Ex Vivo and In Vivo Monitoring and Characterization of Thermal Lesions by High-Intensity Focused Ultrasound and Microwave Ablation Using Ultrasonic Nakagami Imaging.
IEEE Transactions on Medical Imaging, 37(7), 1701-1710.
- IJH 2018 • S. Zhang, R. Xu, S. Shang, Y. Han, **S. Liu**, T. Xu, C. Gu, X. Zhu, G. Niu, M. Wan. In Vivo Monitoring of Microwave Ablation in a Porcine Model Using Ultrasonic Differential Attenuation Coefficient Intercept Imaging.
International Journal of Hyperthermia, 34(8), 1157-1170.

DISSERTATION, PREPRINTS, WORKSHOPS, AND BOOK CHAPTERS

- Thesis
2026
- **S. Liu.** Loom: Full-Stack Compilation and Automated Exploration of Heterogeneous Multi-Core Spatial Accelerator Systems.
Ph.D. dissertation, University of California, Los Angeles.
- arXiv
2026
- C. Li, Z. Zhang, M. Li, Y. Pang, T. Wu, M. Li, Y. Liu, H. Guo, M. Chen, C. He, K. Ma, W. Xu, S. Han, **S. Liu**, L. Zhu. Humanize MLE Agents: Multi-Agent Session Alternation Beyond Single-Agent Limits.
arXiv:2610.13494.
- arXiv
2026
- **S. Liu**, L. Zhu, Z. Zhang, D. Zou, Z. Zhang, C. Li, S. Bian, S. Han, T. Nowatzki. Humanize: Judgement Engineering for Agentic Coding.
arXiv:2610.08900.
- arXiv
2025
- **S. Liu**, J. Ke, T. Nowatzki, J. Cong. Demystifying FPGA Hard NoC Performance.
arXiv:2503.10861.
- WDDSA
2022
- J. Weng, **S. Liu**, D. Kupsh, T. Nowatzki. A Full-Stack Infrastructure for Automating Spatial Architecture Research.
Workshop on Democratizing Domain-Specific Accelerators (WDDSA), co-located with MICRO.
- LATTE
2021
- J. Weng, V. Dadu, **S. Liu**, T. Nowatzki. Generality is the Key Dimension in Accelerator Design.
Workshop on Languages, Tools, and Techniques for Accelerator Design (LATTE), co-located with ASPLOS.
- Chapter
2021
- Q. Zheng, **S. Liu**, A. E. P. Villa, A. Lintas. Unsupervised Analysis of EEG Signals Reveals Common Personality Traits During an Iterated Ultimatum Game.
Advances in Cognitive Neurodynamics (VII), Springer, pp. 275-276.

HONORS AND AWARDS

- 2022
- **MICRO Best Paper Runner-up.** OverGen.
- 2022
- **IEEE Micro Top Picks.** PolyGraph.
- 2021
- **IEEE Micro Top Picks, Honorable Mention.** DSAGEN.
- 2020
- **IEEE Micro Top Picks.** SPU.
- 2019
- **Dean's Fellowship and University Fellowship.** UCLA.

ACADEMIC SERVICE

- 2021
- Artifact Evaluation Committee, HPCA 2021.
- 2021–2026
- Journal peer reviewer: ACM TACO, ACM TODAES, ACM TRETs, ACM TECS, IEEE TC, IEEE TCAD, IEEE TVLSI, IEEE CAL, IEEE JETCAS, Journal of Systems Architecture, Journal of Signal Processing Systems.

TECHNICAL SKILLS

- **Programming:** C, C++, Rust, Python, Scala, MATLAB.
- **Hardware:** Chisel, Verilog, SystemVerilog; RTL design and verification; FPGA prototyping.
- **Compilers and simulation:** LLVM, MLIR, CIRCT, gem5, Chipyard, Rocket Chip, FireSim.
- **EDA tools:** Synopsys VCS, Design Compiler, IC Compiler; Verilator; AMD Vivado and Vitis.

EARLIER HONORS AND COMPETITIONS

- 2017
- Finalist, Interdisciplinary Contest in Modeling.
- 2017
- First Prize, China Big Data Modeling Contest.
- 2016
- First Prize, Data Modeling Contest, XJTU.
- 2016
- First Prize, Mathematical Modeling Contest, XJTU.